Amendments to the Specification:

Please replace paragraph 8 with the following amended paragraph:

In an alternative specific embodiment, the invention provides an alternative method for forming a self aligned contact region for a dynamic random access memory device. The method includes providing a semiconductor substrate, ~~which ahs a cell~~ which has a cell region and a peripheral region. The method forms at least a first gate structure, a second gate structure, a third gate structure, and a fourth gate structure in the cell region and forms a gate structure in the peripheral region. Each of the gate structures has an overlying cap layer, which protects it. The second gate structure is spaced by a bit line region to the third gate structure. The first gate structure is spaced by a first capacitor contact region to the second gate structure. The third gate structure is spaced by a second capacitor contact region to the fourth gate structure. The method forms a conformal dielectric layer overlying the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, the bit line region, the first capacitor contact region, and the second capacitor contact region in the cell region and the gate structure in the peripheral region. The method includes forming an interlayer dielectric material overlying the conformal dielectric layer and planarizing the interlayer dielectric material. A masking layer is formed overlying the planarized interlayer dielectric material. The method exposes a continuous common region within a portion of the planarized interlayer dielectric material overlying the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, the bit line region, the first capacitor contact region, and the second capacitor contact region while maintaining the planarized interlayer dielectric material overlying the gate structure in the peripheral region. The method includes performing an etching process to remove the exposed portion of the planarized interlayer dielectric layer in the continuous common region to expose the bit line contact, the first capacitor contact region, and the second capacitor contact region while using portions of the conformal layer as a mask to prevent any conductive portions of the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure from being exposed. The method deposits a polysilicon fill material within the continuous common region and overlying the bit line region, the first capacitor contact region, and the

second capacitor region, the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure to a predetermined thickness. The polysilicon fill material is planarized to reduce the predetermined thickness and to simultaneously reduce a thickness of a portion of the interlayer dielectric material to a vicinity of an upper region of the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, and the gate structure. The method continues the planarization of the polysilicon fill material and the interlayer dielectric material to expose a portion of the first gate structure, a portion of the second gate structure, a portion of the third gate structure, a portion of the fourth gate structure, and a portion of the gate structure while leaving portions of the polysilicon fill material on the bit line region, the first capacitor contact region and the second capacitor contact region. The polysilicon fill material on the first capacitor contact region is isolated from the polysilicon fill material on the bit line region and the polysilicon fill material on the second capacitor contact region is isolated from the polysilicon fill material on the bit line region.

Please replace paragraph 9 with the following amended paragraph:

Many benefits are achieved by way of the present invention over conventional techniques. For example, the present technique provides an easy to use process that relies upon conventional technology. In some embodiments, the method provides higher device yields in dies per wafer. Additionally, the method provides a process that is compatible with conventional process technology without substantial modifications to conventional equipment and processes. Preferably, the invention provides for an improved process integration for design rules of ~~0.13 microns and less~~ 0.13 microns or less. Additionally, pitch between the transistor gate structures can be less than 0.135 microns. Preferably, the invention provides a self-aligned contact formation process for DRAMs and other integrated circuit devices. Depending upon the embodiment, one or more of these benefits may be achieved. These and other benefits will be described in more throughout the present specification and more particularly below.

Please replace paragraph 29 with the following amended paragraph:

Figures 1 through 9 illustrate a method for forming an interconnect structure for a dynamic random access memory device according to an embodiment of the present invention. These diagrams are merely examples, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. We will explain the present method using two cross-sectional view diagrams including a cell array cross-section 100 and a peripheral cross-section 103. A top-view diagram 101 of the cell array cross section is also shown. As shown, the method begins providing a ~~semiconductor~~ substrate 105, ~~e.g.~~ an example of the substrate is a semiconductor wafer. In a specific embodiment, the ~~The~~ substrate is a P-type silicon wafer, but can be others. The substrate includes an overlying oxide layer 107, which has a patterned nitride layer 109. The patterned nitride layer has patterned photoresist mask 111. Certain process details are provided as follows:

Please replace paragraph 41 with the following amended paragraph:

A masking layer 701 is formed overlying the planarized interlayer dielectric material 700 as illustrated by Figure 7. The masking layer exposes a continuous common region 703 within a portion of the planarized interlayer dielectric material overlying the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, the bit line region, the first capacitor contact region, and the second capacitor contact region while maintaining the planarized interlayer dielectric material overlying the gate structure in the peripheral region. That is, the masking layer covers and protects the interlayer dielectric material and underlying structures in the peripheral region, as shown. The method includes performing an etching process to remove 703 the exposed portion of the planarized interlayer dielectric layer in the continuous common region to expose the bit line contact, the first capacitor contact region, and the second capacitor contact region while using portions of the conformal layer as a mask to prevent any conductive portions of the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure from being exposed. As shown, the conformal layer has been removed from contact regions, e.g., bit line, capacitor. As also shown, the interlayer dielectric material still remains over portions of the first gate structure and the second gate structure. Also, portions of the conformal layer and cap layer act as stop layers for each of the

gate structures to prevent conductive regions of the gate structures from being exposed in certain embodiments. A simplified top view of a plurality of cells 705 in a cell array is also shown.

Please replace paragraph 43 with the following amended paragraph:

The polysilicon fill material is planarized 900 to reduce the predetermined thickness of the polysilicon material, as illustrated by Figure 9. Planarization also simultaneously reduces a thickness of a portion of the interlayer dielectric material to level within a vicinity of an upper region of the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, and the gate structure. The method continues the planarization of the polysilicon fill material and the interlayer dielectric material to expose a portion of the first gate structure, a portion of the second gate structure, a portion of the third gate structure, a portion of the fourth gate structure, and a portion of the gate structure while leaving portions of the polysilicon fill material on the bit line region, the first capacitor contact region and the second capacitor contact region. The polysilicon fill material on the first capacitor contact region is isolated from the polysilicon fill material on the bit line region and the polysilicon fill material 901 on the second capacitor contact region is isolated from the polysilicon fill material on the bit line region. As also shown, the interlayer dielectric material has a thickness that is substantially the same as the gate structures (903 shown as an example of a gate structures) and portions of polysilicon fill material. Depending upon the embodiment, there can be many variations, alternatives, and modifications.